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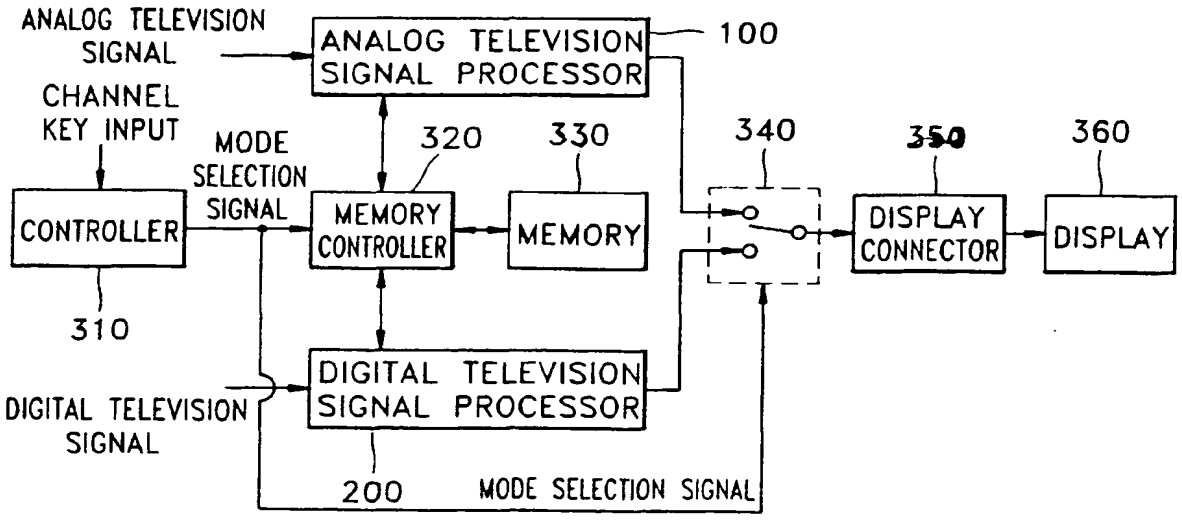
(54) Receiver having analog and digital video modes and receiving method thereof

(57) In a receiver having both an analog video service mode and a digital video mode and a receiving method thereof, when the analog video mode is selected according to a mode selection signal indicating that a television channel is for the analog video mode or the digital video mode, a large-capacity memory used for the digital video-decoding may also be used as a frame memory for Y/C separation and post-processing, for enhancing picture quality, improving the efficiency of the memory and reducing the cost of a system.

FIG. 5



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Description

The present invention relates to a receiver having analog and digital video modes and a receiving method thereof, and more particularly, to a receiver sharing a memory for digital television signal processing in an analog video mode, and to a receiving method thereof.

The digital video mode is to receive television signals digital-processed by the MPEG (Moving Picture Experts Group) standard from a transmitter such as a broadcasting station, and the analog video mode is to receive signals analog-processed by a conventional broadcasting method such as NTSC, PAL or SECAM. Meanwhile, a set-top-box for decoding a bitstream coded by MPEG-2, or a digital television including a set-top-box are developed, conventional analog video service is still overwhelmingly predominant. In answer to this situation, a television receiver having both analog and digital video modes is adopted. Such an analog and digital video mode television receiver requires 8-32Mb of memory for digital television signal decoding. This memory, however, is idle (i.e., unused) when the analog video mode is selected.

In an analog receiver having the analog video mode, as shown in Figure 1, a tuner 11 selects a desired television channel signal among received analog television channel signals, to output an intermediate frequency signal. A channel demodulator 12 amplifies and demodulates the intermediate frequency signal of the channel selected by tuner 11. (Here, though the amplified and demodulated signal is separated into audio and video signals, only the video portion will be described for the sake of simplifying the drawings and specification.) A luminance/ chrominance (Y/C) separator 13 separates the video signal output from channel demodulator 12 into luminance (Y) and chrominance (C) signals, using a correlation between a current line and its adjacent ones and/or between the previous frame and current frame stored in a frame memory 14. The separated signals are stored in frame memory 14 and at the same time input to the display connector 15.

The display connector 15 converts the Y and C signals received from Y/C separator 13 into analog R, G and B signals and then outputs the converted signals to a display 16 which is, for example, a picture tube.

Tuner 11, channel demodulator 12, Y/C separator 13 correspond to an analog television signal processor 100. Further, there can be included an analog-to-digital converter for converting the output of channel demodulator 12 into digital form in order to store it in frame memory 14 as digital data, and a digital-to-analog converter for converting the output of display connector 15 into analog form in order to display it as an analog signal on display 16.

When a comb filter is used for the Y/C separation in a conventional analog television, a cross color or cross luminance phenomenon occurs due to insufficient Y/C separation. Accordingly, as shown in the circuit of Figure 1, a frame memory is used for three-dimensional Y/C separation often noted as frame comb filtering, to enhance picture quality.

Frame memory 14 may be also used for post-processing, for further enhancement of the picture quality after the Y/C separation. That is, edge components determined by the correlation between a current frame and a previous frame using frame memory 14, are emphasized. Most such methods for enhancing picture quality require a costly high-capacity memory. Therefore, a method incorporating a limited memory is generally used, even though it is not so effective.

Figure 2 is a schematic block diagram of a conventional digital television for receiving television signals coded by MPEG-2. In Figure 2, a tuner 21 selects a desired channel signal from television signals received from an antenna. Here, the television signals received from the antenna are input in an MPEG-2 packet structure.

That is, according to an MPEG-2 format, the transmitting data has a system layer structure consisting of packets of a 188-byte unit. The packet structure includes a header having sync and side information and another region having audio data, video data and user data. The video data is compressed by an inter-picture encoding or intra-picture encoding technique. Here, during the inter-picture encoding of predicted- and bi-directionally predicted picture data within each group of pictures (GOP) unit (fifteen pictures maximum) following an intra-picture, only the differences between the picture being encoded and another picture are encoded. Here, each GOP includes intra-picture data which can be independently coded without reference to any other picture data, predicted-picture data which can be coded from the preceding intra-picture data and the preceding predicted- pictures data by using motion compensation between adjacent pictures, and bi-directionally predicted picture data which can be coded from a preceding intra- or predicted-picture data and the following intra- or predicted-picture data, using motion compensation, between adjacent pictures.

A channel demodulator 22 including a quadrature phase shift-keying demodulator, a Reed-Solomon decoder and a Viterbi decoder, converts a desired digital television channel signal which is output from tuner 21, into an MPEG-2 bitstream.

A system decoder 23 separates the MPEG-2 bitstream into audio and video data streams. (Here, as in the case of Figure 1, the audio portion will not be described, though it is assumed that an audio decoder and audio signal processor are provided for decoding and signal-processing the audio stream, and only the video signal process is shown and will be described.)

A video decoder 24 includes a variable-length decoder for variable-length-decoding the video data stream output from system decoder 23, an inverse quantizer for inverse quantizing the variable-length-decoded data, an inverse discrete cosine transform (IDCT)

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operator for performing IDCT operation, and motion compensator for computing motion-predicted data. Video decoder 24 reconstructs the compressed data in order to display the original data on a display 27. Here, the reconstructed video is converted into an analog RGB signal by display connector 26 before being displayed on display 27.

A memory 25 is used for video-decoding, i.e., source-decoding, the digital video data performed in video decoder 24.

That is, memory 25 includes a video buffering verifier (VBV) buffer (also called a channel buffer) for converting the constant bit rate of the video data stream output from system decoder 23 into a variable bit rate before variable-length-decoding, and frame buffers for reconstructing the predicted and bi-directionally predicted pictures after compensating for motion by adding block data obtained by reading out a predetermined size of DCT blocks corresponding to a motion vector from previous frame data and inverse-DCT data. Accordingly, memory 25 requires a capacity of 8Mb to 32Mb for the frames and VBV buffers in order to decode the video data stream.

Here, tuner 21, channel demodulator 22, system decoder 23 and video decoder 24 correspond to a digital television signal processor 200. Further, the combination of digital television signal processor 200 and memory 25 is generally called a set top box (STB).

Since it is expected that analog TV services such as NTSC, PAL will continue to exist, a consumer television system must have capability to display both analog and digital video services. Two methods therefor will be described as follows.

Referring to Figure 3, all processes for digital video services are performed in an STB 210 and then the reconstructed video signal is applied to a video input terminal of a conventional analog television 110. Accordingly, digital video service can be received in the analog television 110 also.

Referring to Figure 4, a television having a conventional analog video mode is provided with the digital television signal processor 200 and the memory 25, to thereby receive both analog video service and digital video service.

Accordingly, as shown in Figures 3 and 4, the memory is used for analog television signal processing, i.e., Y/C separation and post-processing, and an 8-32Mb memory is used for decoding of digital video. When a television receives only analog video service, the memory of an 8-32Mb for digital video-decoding is not used. It is thus inefficient because an existing resource within the television system cannot be used.

Accordingly, it is an aim of embodiments of the present invention to provide a receiver having analog and digital video modes, wherein a memory required for digital video signal decoding is commonly used for analog television signal processing in an analog video mode.

It is another aim to provide a receiving method wherein a memory required for decoding a digital video signal is commonly used for analog television signal processing in an analog video mode.

According to a first aspect of the invention, there is provided a receiver having an analog video mode for receiving television signals analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signals digital-processed by a predetermined digital signal format, the receiver comprising: first signal processing means, for processing the received analog television signals; second signal processing means, for decoding the received digital television signal; a memory for storing data in order to decode the digital TV signal in said second signal processing means and process digitized analog television signal in said first signal processing means; generating means, for generating a mode selection signal which represents either said analog video mode or said digital video mode; and a memory controller, for controlling said memory according to said mode selection signal in order to write/read the signal processed in said first signal processing means, to/from said memory, during said analog video mode and write/read the digital TV signal to/from during said digital video mode.

Preferably, said first signal processing means, comprises a first tuner, for selecting a desired channel among received analog television channels, to output an intermediate frequency signal of said selected channel; a first channel demodulator for amplifying and demodulating said intermediate frequency signal of the channel selected by said first tuner, to output a video signal; and a luminance/chrominance separator for separating the luminance (Y) signal and the chrominance signal (C) from video signals output from said first channel demodulator, using a correlation between adjacent pictures stored in said memory and/or between adjacent lines stored in said memory.

The receiver preferably further comprises a post-processor for post-processing using said separated luminance signal for enhancing picture quality.

Said memory controller may include switching means for selecting one of the outputs from said first and second signal processing means according to said mode selection signal to write in said memory and supply data stored in said memory to said selected signal processing means.

Said switching means preferably includes at least one multiplexer.

Preferably, switching means are provided for selecting one of the output signals from said first signal processing means and said second signal processing means according to said mode selection signal; and display controlling means are provided for displaying the signal selected by said switching means on a display.

According to a second aspect of the invention, there is provided a receiver having an analog video mode for receiving television signals analog processed by a pre-

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determined analog broadcasting method and a digital video mode for receiving television signals digital-processed by a predetermined digital signal format, the receiver comprising: controlling means connected to common bus lines having a data line or multiple of data lines and a clock line for generating mode selection data which represents either said analog video mode or said digital video mode wherein first signal processing means is connected to said common bus lines, for signal-processing the analog television signal received according to the mode selection data, second signal processing means is connected to said common bus lines, for decoding the digital television signal received according to the mode selection data and a memory is connected to said common bus lines, for decoding the digital television signal from said second signal processing means, storing data processed in said first signal processing means according to said mode selection data for representing analog video service mode, and supplying the stored data to said first signal processing means.

Said first signal processing means may comprise a first tuner for selecting a desired channel among received analog television channels, to output an intermediate frequency signal; a first channel demodulator for amplifying and demodulating said intermediate frequency signal of the channel selected by said first tuner to output a video signal; and a luminance/chrominance separator for separating video signal output from said first channel demodulator into luminance (Y) signal and chrominance (C) signal using correlation between adjacent pictures stored in said memory and between adjacent lines stored in said memory.

A post-processor may be provided for post-processing said separated luminance signal for enhancing picture quality.

In said analog video mode, said memory is preferably used as a frame memory for storing data output from said first channel demodulator in a picture unit.

In said analog video mode, said memory may be used as a frame memory for storing data output from said first channel demodulator in a picture unit and data input from said post-processor in a picture unit.

Said first signal processing means may comprise: a first tuner for selecting a desired channel among received analog television channels, to output an intermediate frequency signal; a first channel demodulator for amplifying and demodulating said intermediate frequency signal of the channel selected by said first tuner and outputting a video signal; and a post-processor for post-processing using video signal output from said first channel demodulator and data stored in said memory.

In said analog video mode, said memory may be used as a frame memory for storing data output from said first channel demodulator in a picture unit.

Preferably, said second signal processing means comprises: a second tuner for selecting a desired channel signal among received television signals coded by the digital signal format; a second channel demodulator for channel-decoding the desired channel signal output from said second tuner; a system decoder for outputting a video data stream from the channel-decoded signal output from said second channel demodulator; and a video decoder for reconstructing video data from said video data stream.

In said digital video mode, said memory may be used as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate for video-decoding and as a frame buffer for motion compensation.

Switching means may be provided for selecting one of the output signals from said first signal processing means and said second signal processing means according to said mode selection data; and display control means provided for displaying the signal selected by said switching means on display.

According to a third aspect of the invention, there is provided a receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined digital signal format, comprising: a first input terminal for receiving digitized analog television signal; a second input terminal for receiving channel-decoded digital television signal; a generator for generating a mode selection signal which represents either said analog video mode or said digital video mode; a memory for storing data in order to video-decode said channel-decoded digital television signal; a microprocessor for processing one of the signals input into said first and second input terminals according to said mode selection signal, and for controlling said memory so that said memory is shared by writing/reading the digitized analog signal which is input into said first input terminal to/from said memory in said analog video mode; and display controlling means for controlling the signal processed by said microprocessor so as to display the signal on a display.

The receiver may further comprise a system decoder for extracting video data stream from channel-decoded digital television signal input into said second input terminal.

Preferably, said microprocessor performs luminance/chrominance separation of the digitized analog television signal input into said first input terminal, in said analog video mode, and reconstructing digital video signal from the video data stream output from said system decoder, in said digital video mode.

Said microprocessor may perform luminance/chrominance separating the digitized analog television signal which is input into said first input terminal, in said analog video mode, and performs system decoding, in said digital video mode, to thereby extract video data stream from the channel-decoded digital television signal input into said second input terminal.

A video decoder may be provided for reconstructing

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digital video signal from the video data stream output from said microprocessor.

Said microprocessor preferably performs luminance/chrominance separation of the digitized analog television signal input into said first input terminal in said analog video mode, and extracts video data stream from the channel-decoded digital television signals input into said second input terminal, and reconstructs digital video signal from the extracted video data stream in said digital video mode.

The receiver may further comprise a system and video decoder for extracting a video data stream from the channel-decoded digital television signal input into said second input terminal and reconstructing digital video signal from the extracted video data stream.

Said microprocessor preferably performs luminance/chrominance separation of the digitized analog television signals input into said first input terminal, in said analog video mode, and writes and reads said digital television signal to and from said memory for system-decoding and video-decoding, in said digital video mode.

Said microprocessor may perform post-processing using separated luminance signal.

Preferably, said memory is used as a frame memory for luminance/chrominance separation of the digitized analog television signal, in said analog video mode.

Said memory may be used as a frame memory for luminance/chrominance separation and post-processing, in said analog video mode.

Said memory may be used as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer.

Said microprocessor may post-process digitized analog television signal input into said first input terminal, in said analog video mode, and reconstruct digital video signal output from said system decoder, in said digital video mode.

Preferably, said microprocessor performs post-processing of the digitized analog television signal input into said first input terminal, in said analog video mode, and system-decoding of the channel-decoded digital television signal input into said second input terminal, in said digital video mode, to thereby extract video data stream.

Said microprocessor may further comprise a video decoder for reconstructing said video data stream from said digital video signal.

Said microprocessor preferably performs post-processing of the digitized analog television signal input into said first input terminal, in said analog video mode, and system-decoding of the channel-decoded digital television signal input into said second input terminal, in said digital video mode, to thereby extract video data stream, and reconstructs digital video signal from the extracted video data stream.

The receiver may further comprise a system and video decoder for extracting video data stream from channel-decoded digital television signal input into said second input terminal and reconstructing video data from the extracted video data stream.

Preferably, said microprocessor performs post-processing of the digitized analog television signal input into said first input terminal, in said analog video mode, and writes and reads said digital television signal to and from said memory for system-decoding and video-decoding, in said digital video mode.

Said memory may be used as a frame memory for post-processing, in said analog video mode.

Said memory may be used as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer, in said digital video mode.

According to a fourth aspect, there is provided a receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined format, comprising: a first input terminal for receiving a channel-demodulated analog TV signal; a second input terminal for receiving a channel-decoded digital TV signal; a generator for generating a mode selection signal which represents either said analog video mode or said digital video mode; a memory for storing data either in a process of source-decoding said channel-decoded digital television signal or in a process of processing said channel-demodulated analog television signal; a microprocessor for writing/reading said digital television signal during said digital video mode or said digitized analog television signal during said analog video mode, to and from said memory according to said mode selection signal; analog processing means having an input terminal for receiving said channel-demodulated analog television signal, an input terminal for receiving data read from said memory through said microprocessor, an output terminal for outputting data to said microprocessor to store said data into said memory and an output terminal for outputting processed analog television signal; digital processing means having an input terminal for receiving said channel-decoded digital television signal, input and output terminals connected to said microprocessor, and a terminal for outputting said video signal reconstructed from said channel-decoded digital television signal; switching means for selecting one of said reconstructed digital video signal and said processed analog television signal according to said mode selection signal; and display controlling means for controlling the signal output from said switching means to display the signal on a display.

Said digital processing means preferably extracts video data stream from said channel-decoded digital television signal by system decoding, and reconstructs digital video signal from said extracted video data stream.

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Said digital processing means may extract video data stream from said channel-decoded digital television signal, reconstructs digital video signal from said extracted video data stream, and converts said reconstructed digital video signal into analog video signal.

Preferably, said memory is used as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer, in said digital mode.

Said analog processing means may perform luminance/chrominance separation of said channel-demodulated analog television signal.

In said analog video mode, said memory is preferably used as a frame memory for luminance/chrominance separation of said channel-demodulated analog television signal.

According to a fifth aspect of the invention, there is provided a receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined format, comprising: a first input terminal for receiving a channel-demodulated analog TV signal; a second input terminal for receiving a channel-decoded digital TV signal; a generator for generating a mode selection signal which represents either said analog video mode or said digital video mode; a memory for storing data in a process of either video-decoding of said channel-decoded digital television signal or in a process of processing said channel-demodulated analog television signal; a microprocessor having an input terminal for receiving said channel-decoded digital television signal, reconstructing digital video signal from said digital television signal in said digital video mode and for writing/reading said digital television signal during said digital video mode or said digitized analog television signal during said analog video mode, to and from said memory according to said mode selection signal; analog processing means having an input terminal for receiving said channel-demodulated analog television signal, an input terminal for receiving data read from said memory through said microprocessor, an output terminal for outputting data to said microprocessor to store said data into said memory and an output terminal for outputting processed analog television signal; digital processing means for converting said reconstructed digital video signal output from said microprocessor into analog signal; switching means for selecting one of said reconstructed digital video signal from said microprocessor and said processed analog television signal; and display controlling means for controlling the signal output from said switching means to display the signal on a display.

Preferably, said microprocessor multiplexes said channel-decoded digital television signal, extracts video data stream from said channel-decoded digital television signal by system-decoding, and reconstructs said digital video signal from said extracted video data stream.

The receiver may further comprise a digital processing means for converting reconstructed digital video signal output from said microprocessor into analog signals and then supplying the converted analog signal to said switching means.

Said display controlling means preferably converts said switched signal into analog signal.

Said memory may be used as a buffer for temporarily storing said channel-demodulated analog television signal, as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer.

According to a sixth aspect of the present invention, there is provided a receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined format, comprising: a first input terminal for receiving a channel-demodulated analog TV signal; a second input terminal for receiving a channel-decoded digital TV signal; a generator for generating a mode selection signal which represents either said analog video mode or said digital video mode; a memory for storing data either in a process of source-decoding said channel-decoded digital television signal or in a process of processing channel-demodulated said analog television signal; a microprocessor having an input terminal for receiving said channel-decoded digital television signal, extracting video data stream from said channel-decoded digital television signal in said digital video mode, and for writing/reading said digital television signal during said digital video mode or said digitized analog television signal during said analog video mode, to/from said memory according to said mode selection signal; analog processing means having an input terminal for receiving said channel-demodulated analog television signal, an input terminal for receiving data read from said memory through said microprocessor, an output terminal for outputting data to said microprocessor to store said data into said memory, and an output terminal for outputting processed analog television signal; digital processing means for reconstructing digital video signal from said video data stream; switching means for selecting one of output signal of said digital processing means and said processed analog TV signal; and display controlling means for controlling the signal output from said switching means to display the signal on a display.

Preferably, said microprocessor multiplexes said channel-decoded digital television signal and extracts video data stream from said channel-decoded digital television signal.

Said digital processing means may convert reconstructed digital video signals into analog signal.

Said display controlling means may convert the signal switched in said switching means into analog signal.

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Preferably, said memory is used as a buffer for temporarily storing said channel-demodulated analog television signal, as a channel buffer for converting a transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer, in said digital video mode.

Preferably, said analog processing means performs luminance/chrominance separation of said channel-demodulated analog television signal.

Said memory may be used as a frame memory for luminance/chrominance separation of said channel-demodulated analog television signal, in said analog video mode.

Said analog processing means preferably performs post-processing of said channel-demodulated analog television signal.

Said memory may be used as a frame memory for post-processing of said channel-demodulated analog television signal, in said analog video mode.

Preferably, said analog processing means performs luminance/chrominance separation and post-processing of said channel-demodulated analog television signal.

Said memory may be used as a frame memory for luminance/chrominance separation and post-processing of said channel-demodulated analog television signal, in said analog video mode.

According to a seventh aspect of the invention, there is provided a receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined format, comprising: a first input terminal for receiving a channel-demodulated analog TV signal; a second input terminal for receiving a channel-decoded digital TV signal; a generator for generating a mode selection signal for representing said analog video mode and said digital video mode; a memory for storing data in a process of either source-decoding said channel-decoded digital television signal or processing channel-demodulated said analog television signal; digital processing means including an input terminal for receiving said channel-decoded digital television signal and for extracting video data stream from said channel-decoded digital television; a microprocessor for inputting video data stream extracted from said digital processing means, thereby reconstructing digital video signal, and writing and reading digitized analog television signal to/from said memory in analog video mode; analog processing means having an input terminal for receiving said channel-demodulated analog television signal, an input terminal for receiving data read from said memory through said microprocessor, an output terminal for outputting data to said microprocessor to store said data into said memory, and an output terminal for outputting processed analog television signal; switching means for selecting one of output signal of said digital processing means and said processed analog TV signal; and display controlling means for controlling the signal output from said switching means to display the signal on a display.

The receiver may further comprise converting means for converting digital video signal reconstructed in said microprocessor into analog signal and then supplying the converted analog signal to said switching means, where the signal output from said analog processing means is an analog signal.

Said display controlling means preferably converts the signal switched in said switching means into analog signal, where the switched signal is a digital signal.

Said memory may be used as a channel buffer for converting a transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer, in said digital video mode.

Said analog processing means preferably performs luminance/chrominance separation of said channel-demodulated analog television signal.

Said memory may be used as a frame memory for luminance/chrominance separation of said channel-demodulated analog television signal, in said analog video mode.

Said analog processing means may perform post-processing of said channel-demodulated analog television signals.

Said memory is preferably used as a frame memory for post-processing of said channel-demodulated analog television signal, in said analog video mode.

Said analog processing means preferably performs luminance/chrominance separation and post-processing said channel demodulated analog television signal.

Said memory may be used as a frame memory for luminance/chrominance separation and post-processing of said channel-demodulated analog television signal, in said analog video mode.

According to an eight aspect of the invention, there is provided a method for receiving television signal analog-processed by a predetermined analog broadcasting method and television signal digital-processed by a predetermined digital signal format, comprising the steps of: (a) generating a mode selection signal to determine whether a channel selected by a user is a television channel of an analog video mode or a television channel of a digital video mode; and (b) storing digital television signal received according to said mode selection signal in a memory for digital video decoding, and decoding using the data stored in said memory.

According to a ninth aspect of the present invention, there is provided a method for receiving television signal analog-processed according to a predetermined analog broadcasting method and television signal digital-processed by a predetermined digital signal format, comprising the steps of: (a) generating a mode selection signal to determine whether a channel selected by a user is a television channel of an analog video mode or a television channel of a digital video mode; and (b) storing an-

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alog television signal received according to said mode selection signal in a memory for digital video decoding, and reading the data stored in said memory to process the data in said memory in said analog video mode.

According to a tenth aspect of the present invention, there is provided a method for receiving television signal analog-processed according to a predetermined analog broadcasting method and television signal digital-processed by a predetermined digital signal format, comprising the steps of: (a) generating a mode selection signal to determine whether a channel selected by a user is a television channel of an analog video mode or a television channel of a digital video mode; and (b) storing received digital television signal according to said mode selection signal in a memory for digital video-decoding and decoding the data stored in said memory in said digital video mode, and storing received analog television signal in said memory for digital video-decoding and reading the data stored in said memory to process the data in said memory in said analog video mode.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of a conventional analog television;

Figure 2 is a block diagram of a conventional digital television;

Figure 3 is a schematic diagram of the conventional analog television with STB;

Figure 4 is a schematic diagram of a digital television having a conventional analog video mode;

Figure 5 is a block diagram of a receiver having analog and digital video modes according to a first embodiment of the present invention;

Figure 6 is a detail view of the memory controller shown in Figure 5;

Figure 7 is a block diagram of the receiver having analog and digital video modes according to a second embodiment of the present invention;

Figure 8 is a block diagram of the receiver having analog and digital video modes according to a third embodiment of the present invention;

Figures 9A through 9C are modifications of the third embodiment shown in Figure 8;

Figure 10 is a block diagram of the receiver having analog and digital video modes according to a fourth embodiment of the present invention;

Figure 11 is a detail block diagram of an analog processor shown in Figure 10; and

Figures 12A through 12C are modifications of the fourth embodiment shown in Figure 10.

Figure 5 is a block diagram of a receiver having analog and digital video modes according to a first embodiment of the present invention.

Here, as the structure and operation of the analog and digital television signal processors 100 and 200 in Figure 5 are the same as those in Figures 1 and 2, no further description will be given.

Referring to Figure 5, a controller 310 determines whether an input channel key is a television channel processed by a conventional analog method (an analog television channel) or a television channel digital-encoded by MPEG-2 (a digital television channel), and outputs to a memory controller 320 a mode selection signal for either an analog or digital video mode. According to the mode selection signal, memory controller 320 then selects one output among those processed in analog television signal processor 100 and digital television signal processor 200, to store the selected output in a memory 330, or read the data stored in memory 330 to supply the data to either analog television signal processor 100 or digital television signal processor 200.

Here, in the analog video mode signal processed in analog television signal processor 100 is displayed on a display 360 through a multiplexer 340 and a display connector 360, and in the digital video mode signal processed in digital television signal processor 200 is displayed on display 360 through multiplexer 340 and display connector 350.

Here, multiplexer 340 supplies video signal selected according to a mode selection signal output from controller 310 to display connector 350.

In the analog video mode, memory 330 is used as the frame memory (or a field memory) for the Y/C separation and post-processing as described referring to Figure 1. In the digital video service mode, on the other hand, memory 330 is used as the VBV buffer for converting the transmission rate and as the frame buffer for motion compensation, as described referring to Figure 2.

Figure 6 is a detail view of the memory controller 320 shown in Figure 5.

Referring to Figure 6, input and output lines include a data line for reading or writing data to and from memory 330, an address line and a memory control line such as an enable. Here, memory controller 320 includes a plurality of multiplexers 320.1-320.n for switching, wherein first input terminals a1-an of each multiplexer are respectively connected to the input/output (I/O) lines of digital television signal processor 200, second input terminals c1-cn are respectively connected to the I/O lines of analog television signal processor 100, and fixed terminals b_1-b_n are respectively connect to the I/O lines

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of memory 330.

Accordingly, input and output lines of memory 330 are connected to input and output lines of digital television signal processor 200 when the mode selection signal indicates the analog video mode, in order to use memory 330 as a frame buffer for Y/C separation and post-processing. Conversely, input and output lines of memory 330 are connected to input and output lines of digital television signal processor 200 when the mode selection signal indicates the digital video mode, in order to use memory 330 as the VBV buffer for converting transmission rate and as the frame buffer for motion compensation.

Meanwhile, in Figure 7, a receiver sharing a memory for both analog and digital modes using a bus-control method, is shown.

In the bus-control method, function control portions are connected to a controller (microcomputer) through two common bus lines, i.e., data and clock lines, which allow bi-directional data transmission and are connected to one or more data output terminals and a clock output terminal of the controller. When the controller transmits an address and data over the bus lines and the transmitted address corresponds to that of a given function control unit, the address function control unit is operated in accordance with the transmitted data. Accordingly, the bus-control method reduces the burden of the controller and decreases signal-processing time.

Referring to Figure 7, a controller 410 determines whether an input channel key is an analog television channel or a digital television channel. When the selected channel is an analog television channel, controller 410 transmits the corresponding mode selection data via the data line to analog television signal processor 100 and a memory 420 in order to operate analog television signal processor 100 and memory 420, and when the selected channel is a digital television channel, controller 410 transmits the corresponding mode selection data via the data line to digital television signal processor 200 and memory 420 in order to operate digital television signal processor 200 and memory 420.

Memory 420 is used as the frame memory for the Y/C separation and post-processing when the analog video mode is selected, where current frame data processed in analog television signal processor 100 is written in memory 420 through data lines, and previous frame data stored in memory 420 is transmitted to analog television signal processor 100 through the data lines. Memory 420 is also used as the VBV buffer for transmission rate conversion and as the frame buffer for motion compensation when the digital video mode is selected, where data processed in digital television signal processor 200 is stored in memory 420 through the data lines, and previous data stored in memory 420 is transmitted to digital television signal processor 200 through the data lines.

Signals processed in analog television signal processor 100 and digital television signal processor 200 according to the mode selection signal output from controller 410, are switched by multiplexer 430 and then displayed on a display 450 through a display connector 440.

Figure 8 is a block diagram of a receiver having analog and digital video modes according to a third embodiment of the present invention. Here, the memory controller carries out the functions of the hardware in Figure 5, that is, the function of selecting analog television signal processor 100 or digital television signal processor 200 according to the mode selection signal, is programmed, and a memory 519 is alternately used for digital video-decoding and analog television signal processing such as Y/C separation and post-processing.

Referring to Figure 8, a first tuner 511 selects only a desired channel signal among analog television channel signals transmitted through an antenna for receiving analog television channels, to output an intermediate frequency signal.

A first channel demodulator 512 amplifies the intermediate frequency signal of the channel selected from the first tuner 511, and outputs a video signal.

An analog-to-digital converter 513 converts the video signal output from first channel demodulator 512 into digital form.

Meanwhile, a second tuner 514 selects a desired channel signal among digital television channel signals coded according to MPEG-2 and transmitted through an antenna for receiving digital television channels. A second channel demodulator 515 outputs the desired digital television channel signal output from second tuner 514 as an MPEG-2 bitstream, and a system decoder 516 extracts only a video data stream from the MPEG-2 bitstream.

A controller 517 determines whether the input channel key is an analog television channel or a digital television channel in order to output a mode selection signal indicating the proper mode, i.e., the analog video mode or the digital video mode.

A microprocessor 518 receives the mode selection signal to select either the output of analog-to-digital converter 513 connected to a first input port or the output of system decoder 516 connected to a second input port. That is, in an analog video mode, microprocessor 518 selects a digitized analog television channel signal output from analog-to-digital converter 513, and then either writes in a memory 519 or reads from memory 519 using the instructions of a predetermined program, to perform Y/C separation and post-processing. Here, memory 519 is used as a frame memory for the Y/C separation and post-processing.

As shown in Figure 8, signals are received using first and second input ports of the microprocessor 518, alternatively, a multiplexer can be connected to a single input port to switch the two inputs in order to use only one input port of the microprocessor 518. The above modifications can be used for embodiments of Figures

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9A through 9C, Figure 10 and Figures 12A through 12C.

A display connector 520 converts digital data output from microprocessor 518 into analog form, to display analog R, G and B signals on display 521. The display connector can be called a signal converter.

Here, microprocessor 518 can calculate at a high speed, but specific functions such as an inverse DCT which requires high-speed operation could be realized by hardware.

Figures 9A through 9C are modifications of the third embodiment shown in Figure 8.

A microprocessor 522 shown in Figure 9A, receives a digitized analog television channel signal which is output from analog-to-digital converter 513 in analog video mode, to thereby perform Y/C separation and post-processing using memory 519 as described in Figure 8.

Also, microprocessor 522 receives MPEG-2 bitstream from second channel demodulator 515 in digital video mode and then a video data stream is extracted from MPEG-2 bitstream under control of controller 517 and output to a video decoder 523. Video decoder 523 reconstructs video data stream from the extracted video data stream.

Here, microprocessor 522 provides a memory connection path so that video decoder 523 uses memory 519 as a VBV buffer, a frame buffer and a display buffer.

A multiplexer 524 selects one of digitized analog signal, which are output from microprocessor 522 according to the mode selection signal output from controller 517 and reconstructed data in video decoder 523.

A microprocessor 525 shown in Figure 9B performs Y/C separation and post-processing in analog video mode as described in Figure 9A, and MPEG-2 system decoding and video-decoding in digital video mode. That is, in the case of digital video mode, video data stream is extracted from MPEG-2 bitstream output from second channel demodulator 515 and then video data is reconstructed from the extracted video data stream by microprocessor 525.

A microprocessor 527 shown in Figure 9C performs memory control function for sharing memory 519 in analog mode and digital video mode and Y/C separation and post-processing in analog mode as described in Figures 9A and 9B.

Meanwhile, in digital video mode, MPEG-2 system decoding and video-decoding are performed by a system and video decoder 526. Also, a multiplexer 528 supplies one of digitized analog signal output from microprocessor 527 according to the mode selection signal of controller 517 and reconstructed video data output from system and video decoder 526, to display connector 520.

Figure 10 is a block diagram of a receiver having analog and digital video modes according to a fourth embodiment of the present invention. Here, operation of a first tuner 611, a first channel demodulator 612, a second tuner 614, a second channel demodulator 615, a system decoder 616, a display connector 620 and a display 621 is the same as that described in Figure 8.

In the third embodiment shown in Figure 8, memory control function is programmed into a microprocessor 618. However, in the fourth embodiment, the analog television signal processing such as three-dimensional Y/C separation or post-processing is performed by an analog processor 613 separated from microprocessor 618. Analog processor 613 is provided with an A/D converter 701, an analog TV signal processor 702 and a D/A converter 703, as shown in Figure 11.

In A/D converter 701, the channel demodulated signal output from first channel demodulator 612 of Figure 10 is converted into digital data. The digital data is then received by an analog TV signal processor 702 and further stored in a memory 619 through microprocessor 618 operated as a memory controller. The analog TV signal stored in memory 619 is used by the analog TV signal processor 702 for Y/C separation or post-processing. The output processed by the analog TV signal processor 702 is temporarily stored in memory 619 until being read out, and is converted into analog signal in D/A converter 703.

Meanwhile, in case of digital video service, MPEG-2 bitstream is decoded into a video data stream in the system decoder 616 and the video data stream is reconstructed to video data by microprocessor 618. The reconstructed data is converted into analog signal by the D/A converter 623.

According to the mode selection signal output from the controller 617 where a mode is determined by a received channel key, a multiplexer 622 selects an analog TV signal processed in the analog processor 613 or an analog video signal output from the D/A converter 623.

Here, display connector 620 of Figure 10 receives data converted into analog signal and then converts the data into R, G and B signals, to thereby output the R, G and B signals to display 621. In a modification thereof, display connector 620 can be realized by uniting one of components of analog processor 613, i.e., a digital-to-analog converter 703 and digital-to-analog converter 623. Here, the multiplexer 622 converts received digital signals into analog signals, and then outputs analog R, G and B signals into display 621. The above modification is applied to Figures 12A, 12B and 12C.

Meanwhile, the embodiment of Figure 10 can be slightly modified depending on the extent of implementing MPEG decoding by software using the microprocessor 618.

Figures 12A through 12C are modifications of the fourth embodiment shown in Figure 10, where functionally identical portions are given by the same reference numerals as those of Figure 10.

The microprocessor 801 shown in Figure 12A performs only control of the memory 619. The MPEG-2 bitstream decoding and video data stream decoding are performed by a system and video decoder 802 in the outside of the microprocessor 801.

A microprocessor 803 shown in Figure 12B per-

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forms both MPEG-2 bitstream decoding and video data stream decoding.

A microprocessor 804 shown in Figure 12C performs MPEG-2 bitstream decoding. However, video data stream decoding is performed by a video decoder 805 external to the microprocessor 804.

According to embodiments of the present invention, when a receiver for receiving both analog video service and digital video service processes a received analog television channel, a large-capacity memory (as that for digital video decoding) is commonly used as a memory for processing an analog television signal, so that memory efficiency is enhanced and system cost is lower.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. A receiver having an analog video mode for receiving television signals analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signals digital-processed by a predetermined digital signal format, the receiver comprising:

   first signal processing means (100), for processing the received analog television signals;

   second signal processing means (200), for decoding the received digital television signal;

   a memory (330) for storing data in order to decode the digital TV signal in said second signal processing means (220) and process digitized analog television signal in said first signal processing means (100):

   generating means (310), for generating a mode selection signal which represents either said analog video mode or said digital video mode; and

   a memory controller (320), for controlling said memory (330) according to said mode selection signal in order to write/read the signal processed in said first signal processing means (100), to/from said memory (330), during said analog video mode and write/read the digital TV signal to/from during said digital video mode.

2. A receiver according to claim 1, wherein said first signal processing means (100), comprises:

   a first tuner (511), for selecting a desired channel among received analog television channels, to output an intermediate frequency signal of said selected channel;

   a first channel demodulator (512) for amplifying and demodulating said intermediate frequency signal of the channel selected by said first tuner (511), to output a video signal; and

   a luminance/chrominance separator for separating the luminance (Y) signal and the chrominance signal (C) from video signals output from said first channel demodulator (512), using a correlation between adjacent pictures stored in said memory (330, 519) and/or between adjacent lines stored in said memory.

3. A receiver according to claim 2, further comprising a post-processor for post-processing using said separated luminance signal for enhancing picture quality.

4. A receiver according to claim 1, wherein said memory controller (320) includes switching means (320.1-320.n) for selecting one of the outputs from said first and second signal processing means (100, 200) according to said mode selection signal to write in said memory (330) and supply data stored in said memory (330) to said selected signal processing means.

5. A receiver according to claim 4, wherein said switching means includes at least one multiplexer.

6. A receiver according to claim 1, further comprising:

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switching means (340, 430, 524, 528, 622) for selecting one of the output signals from said first signal processing means (100, 511-13, 611-13) and said second signal processing means (200, 514-16, 614-16) according to said mode selection signal; and

display controlling means (350, 440, 520, 620) for displaying the signal selected by said switching means on a display (360, 450, 521, 621).

7. A receiver having an analog video mode for receiving television signals analog processed by a predetermined analog broadcasting method and a digital video mode for receiving television signals digital-processed by a predetermined digital signal format, the receiver comprising: controlling means connected to common bus lines having a data line or multiple of data lines and a clock line for generating mode selection data which represents either said analog video mode or said digital video mode wherein first signal processing means is connected to said common bus lines, for signal-processing the analog television signal received according to the mode selection data, second signal processing means is connected to said common bus lines, for decoding the digital television signal received according to the mode selection data and a memory is connected to said common bus lines, for decoding the digital television signal from said second signal processing means, storing data processed in said first signal processing means according to said mode selection data for representing analog video service mode, and supplying the stored data to said first signal processing means.

8. A receiver according to claim 7, wherein said first signal processing means comprises:

a first tuner for selecting a desired channel among received analog television channels, to output an intermediate frequency signal;

a first channel demodulator for amplifying and demodulating said intermediate frequency signal of the channel selected by said first tuner to output a video signal; and

a luminance/chrominance separator for separating video signal output from said first channel demodulator into luminance (Y) signal and chrominance (C) signal using correlation between adjacent pictures stored in said memory and between adjacent lines stored in said memory.

9. A receiver according to claim 8, further comprising a post-processor for post-processing said separated luminance signal for enhancing picture quality.

10. A receiver according to claim 2 or claim 8, wherein, in said analog video mode, said memory is used as a frame memory for storing data output from said first channel demodulator in a picture unit.

11. A receiver according to claim 3 or 9, wherein, in said analog video mode, said memory is used as a frame memory for storing data output from said first channel demodulator in a picture unit and data input from said post-processor in a picture unit.

12. A receiver according to claim 1 or 7, wherein said first signal processing means comprises:

a first tuner for selecting a desired channel among received analog television channels, to output an intermediate frequency signal;

a first channel demodulator for amplifying and demodulating said intermediate frequency signal of the channel selected by said first tuner and outputting a video signal; and

a post-processor for post-processing using video signal output from said first channel demodulator and data stored in said memory.

13. A receiver according to claim 12, wherein, in said analog video mode, said memory is used as a frame memory for storing data output from said first channel demodulator in a picture unit.

14. A receiver according to claim 1 or 7, wherein said second signal processing means comprises:

a second tuner for selecting a desired channel signal among received television signals coded by the digital signal format;

a second channel demodulator for channel-decoding the desired channel signal output from said second tuner;

a system decoder for outputting a video data stream from the channel-decoded signal output from said second channel demodulator; and

a video decoder for reconstructing video data from said video data stream.

15. A receiver according to claim 14, wherein, in said digital video mode, said memory is used as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate for video-decoding and as a frame buffer for motion compen-

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sation.

16. A receiver according to claim 7, further comprising:

switching means for selecting one of the output signals from said first signal processing means and said second signal processing means according to said mode selection data; and

display control means for displaying the signal selected by said switching means on display.

17. A receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined digital signal format, comprising:

a first input terminal for receiving digitized analog television signal;

a second input terminal for receiving channel-decoded digital television signal;

a generator for generating a mode selection signal which represents either said analog video mode or said digital video mode;

a memory for storing data in order to video-decode said channel-decoded digital television signal;

a microprocessor for processing one of the signals input into said first and second input terminals according to said mode selection signal, and for controlling said memory so that said memory is shared by writing/reading the digitized analog signal which is input into said first input terminal to/from said memory in said analog video mode; and

display controlling means for controlling the signal processed by said microprocessor so as to display the signal on a display.

18. A receiver according to claim 17, further comprising a system decoder for extracting video data stream from channel-decoded digital television signal input into said second input terminal.

19. A receiver according to claim 18, wherein said microprocessor performs luminance/chrominance separation of the digitized analog television signal input into said first input terminal, in said analog video mode, and reconstructing digital video signal from the video data stream output from said system decoder, in said digital video mode.

20. A receiver according to claim 17, wherein said microprocessor performs luminance/chrominance separating the digitized analog television signal which is input into said first input terminal, in said analog video mode, and performs system decoding, in said digital video mode, to thereby extract video data stream from the channel-decoded digital television signal input into said second input terminal.

21. A receiver according to claim 20, further comprising a video decoder for reconstructing digital video signal from the video data stream output from said microprocessor.

22. A receiver according to claim 17, wherein said microprocessor performs luminance/chrominance separation of the digitized analog television signal input into said first input terminal in said analog video mode, and extracts video data stream from the channel-decoded digital television signals input into said second input terminal, and reconstructs digital video signal from the extracted video data stream in said digital video mode.

23. A receiver according to claim 17, further comprising a system and video decoder for extracting a video data stream from the channel-decoded digital television signal input into said second input terminal and reconstructing digital video signal from the extracted video data stream.

24. A receiver according to claim 23, wherein said microprocessor performs luminance/chrominance separation of the digitized analog television signals input into said first input terminal, in said analog video mode, and writes and reads said digital television signal to and from said memory for system-decoding and video-decoding, in said digital video mode.

25. A receiver according to claim 19, wherein said microprocessor performs post-processing using separated luminance signal.

26. A receiver according to claim 19, wherein said memory is used as a frame memory for luminance/chrominance separation of the digitized analog television signal, in said analog video mode.

27. A receiver according to claim 25, wherein said memory is used as a frame memory for luminance/chrominance separation and post-processing, in said analog video mode.

28. A receiver according to claim 19, wherein said memory is used as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion com-

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pensation, and as a display buffer.

29. A receiver according to claim 18, wherein said microprocessor post-processes digitized analog television signal input into said first input terminal, in said analog video mode, and reconstructs digital video signal output from said system decoder, in said digital video mode.

30. A receiver according to claim 17, wherein said microprocessor performs post-processing of the digitized analog television signal input into said first input terminal, in said analog video mode, and system-decoding of the channel-decoded digital television signal input into said second input terminal, in said digital video mode, to thereby extract video data stream.

31. A receiver according to claim 30, wherein said microprocessor further comprises a video decoder for reconstructing said video data stream from said digital video signal.

32. A receiver according to claim 17, wherein said microprocessor performs post-processing of the digitized analog television signal input into said first input terminal, in said analog video mode, and system-decoding of the channel-decoded digital television signal input into said second input terminal, in said digital video mode, to thereby extract video data stream, and reconstructs digital video signal from the extracted video data stream.

33. A receiver according to claim 17, further comprising a system and video decoder for extracting video data stream from channel-decoded digital television signal input into said second input terminal and reconstructing video data from the extracted video data stream.

34. A receiver according to claim 33, wherein said microprocessor performs post-processing of the digitized analog television signal input into said first input terminal, in said analog video mode, and writes and reads said digital television signal to and from said memory for system-decoding and video-decoding, in said digital video mode.

35. A receiver according to claim 29, wherein said memory is used as a frame memory for post-processing, in said analog video mode.

36. A receiver according to claim 29, wherein said memory is used as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer, in said digital video mode.

37. A receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined format, comprising:

a first input terminal for receiving a channel-demodulated analog TV signal;

a second input terminal for receiving a channel-decoded digital TV signal;

a generator for generating a mode selection signal which represents either said analog video mode or said digital video mode;

a memory for storing data either in a process of source-decoding said channel-decoded digital television signal or in a process of processing said channel-demodulated analog television signal;

a microprocessor for writing/reading said digital television signal during said digital video mode or said digitized analog television signal during said analog video mode, to and from said memory according to said mode selection signal;

analog processing means having an input terminal for receiving said channel-demodulated analog television signal, an input terminal for receiving data read from said memory through said microprocessor, an output terminal for outputting data to said microprocessor to store said data into said memory and an output terminal for outputting processed analog television signal;

digital processing means having an input terminal for receiving said channel-decoded digital television signal, input and output terminals connected to said microprocessor, and a terminal for outputting said video signal reconstructed from said channel-decoded digital television signal;

switching means for selecting one of said reconstructed digital video signal and said processed analog television signal according to said mode selection signal; and

display controlling means for controlling the signal output from said switching means to display the signal on a display.

38. A receiver according to claim 37, wherein said digital processing means extracts video data stream from said channel-decoded digital television signal

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by system decoding, and reconstructs digital video signal from said extracted video data stream.

39. A receiver according to claim 37, wherein said digital processing means extracts video data stream from said channel-decoded digital television signal, reconstructs digital video signal from said extracted video data stream, and converts said reconstructed digital video signal into analog video signal.

40. A receiver according to claim 37, wherein said memory is used as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer, in said digital mode.

41. A receiver according to claim 37, wherein said analog processing means performs luminance/chrominance separation of said channel-demodulated analog television signal.

42. A receiver according to claim 41, wherein, in said analog video mode, said memory is used as a frame memory for luminance/chrominance separation of said channel-demodulated analog television signal.

43. A receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined format, comprising:

a first input terminal for receiving a channel-demodulated analog TV signal;

a second input terminal for receiving a channel-decoded digital TV signal;

a generator for generating a mode selection signal which represents either said analog video mode or said digital video mode;

a memory for storing data in a process of either video-decoding of said channel-decoded digital television signal or in a process of processing said channel-demodulated analog television signal;

a microprocessor having an input terminal for receiving said channel-decoded digital television signal, reconstructing digital video signal from said digital television signal in said digital video mode and for writing/reading said digital television signal during said digital video mode or said digitized analog television signal during said analog video mode, to and from said memory according to said mode selection signal;

analog processing means having an input terminal for receiving said channel-demodulated analog television signal, an input terminal for receiving data read from said memory through said microprocessor, an output terminal for outputting data to said microprocessor to store said data into said memory and an output terminal for outputting processed analog television signal;

digital processing means for converting said reconstructed digital video signal output from said microprocessor into analog signal;

switching means for selecting one of said reconstructed digital video signal from said microprocessor and said processed analog television signal; and

display controlling means for controlling the signal output from said switching means to display the signal on a display.

44. A receiver according to claim 43, wherein said microprocessor multiplexes said channel-decoded digital television signal, extracts video data stream from said channel-decoded digital television signal by system-decoding, and reconstructs said digital video signal from said extracted video data stream.

45. A receiver according to claim 43, further comprising a digital processing means for converting reconstructed digital video signal output from said microprocessor into analog signals and then supplying the converted analog signal to said switching means.

46. A receiver according to claim 43, wherein said display controlling means converts said switched signal into analog signal.

47. A receiver according to claim 44, wherein said memory is used as a buffer for temporarily storing said channel-demodulated analog television signal, as a channel buffer for converting the transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer.

48. A receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined format, comprising:

a first input terminal for receiving a channel-demodulated analog TV signal;

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a second input terminal for receiving a channel-decoded digital TV signal;

a generator for generating a mode selection signal which represents either said analog video mode or said digital video mode;

a memory for storing data either in a process of source-decoding said channel-decoded digital television signal or in a process of processing channel-demodulated said analog television signal;

a microprocessor having an input terminal for receiving said channel-decoded digital television signal, extracting video data stream from said channel-decoded digital television signal in said digital video mode, and for writing/reading said digital television signal during said digital video mode or said digitized analog television signal during said analog video mode, to/from said memory according to said mode selection signal;

analog processing means having an input terminal for receiving said channel-demodulated analog television signal, an input terminal for receiving data read from said memory through said microprocessor, an output terminal for outputting data to said microprocessor to store said data into said memory, and an output terminal for outputting processed analog television signal;

digital processing means for reconstructing digital video signal from said video data stream;

switching means for selecting one of output signal of said digital processing means and said processed analog TV signal; and

display controlling means for controlling the signal output from said switching means to display the signal on a display.

49. A receiver according to claim 48, wherein said microprocessor multiplexes said channel-decoded digital television signal and extracts video data stream from said channel-decoded digital television signal.

50. A receiver according to claim 48, wherein said digital processing means converts reconstructed digital video signals into analog signal.

51. A receiver according to claim 48, wherein said display controlling means converts the signal switched in said switching means into analog signal.

52. A receiver according to claim 49, wherein said memory is used as a buffer for temporarily storing said channel-demodulated analog television signal, as a channel buffer for converting a transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer, in said digital video mode.

53. A receiver according to claim 43 or 48, wherein said analog processing means performs luminance/chrominance separation of said channel-demodulated analog television signal.

54. A receiver according to claim 53, wherein said memory is used as a frame memory for luminance/chrominance separation of said channel-demodulated analog television signal, in said analog video mode.

55. A receiver according to claim 37, 43 or 48, wherein said analog processing means performs post-processing of said channel-demodulated analog television signal.

56. A receiver according to claim 55, wherein said memory is used as a frame memory for post-processing of said channel-demodulated analog television signal, in said analog video mode.

57. A receiver according to claim 37, 43 or 48, wherein said analog processing means performs luminance/chrominance separation and post-processing of said channel-demodulated analog television signal.

58. A receiver according to claim 57, wherein said memory is used as a frame memory for luminance/chrominance separation and post-processing of said channel-demodulated analog television signal, in said analog video mode.

59. A receiver having an analog video mode for receiving television signal analog-processed by a predetermined analog broadcasting method and a digital video mode for receiving television signal digital-processed by a predetermined format, comprising:

a first input terminal for receiving a channel-demodulated analog TV signal;

a second input terminal for receiving a channel-decoded digital TV signal;

a generator for generating a mode selection signal for representing said analog video mode and said digital video mode;

a memory for storing data in a process of either

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source-decoding said channel-decoded digital television signal or processing channel-demodulated said analog television signal:

digital processing means including an input terminal for receiving said channel-decoded digital television signal and for extracting video data stream from said channel-decoded digital television;

a microprocessor for inputting video data stream extracted from said digital processing means, thereby reconstructing digital video signal, and writing and reading digitized analog television signal to/from said memory in analog video mode:

analog processing means having an input terminal for receiving said channel-demodulated analog television signal, an input terminal for receiving data read from said memory through said microprocessor, an output terminal for outputting data to said microprocessor to store said data into said memory, and an output terminal for outputting processed analog television signal;

switching means for selecting one of output signal of said digital processing means and said processed analog TV signal: and

display controlling means for controlling the signal output from said switching means to display the signal on a display.

60. A receiver according to claim 59, further comprising converting means for converting digital video signal reconstructed in said microprocessor into analog signal and then supplying the converted analog signal to said switching means, where the signal output from said analog processing means is an analog signal.

61. A receiver according to claim 59, wherein said display controlling means converts the signal switched in said switching means into analog signal, where the switched signal is a digital signal.

62. A receiver according to claim 59, wherein said memory is used as a channel buffer for converting a transmission rate of a constant bit rate into a variable bit rate, as a frame buffer for motion compensation, and as a display buffer, in said digital video mode.

63. A converter according to claim 59, wherein said analog processing means performs luminance/chrominance separation of said channel-demodulated analog television signal.

64. A receiver according to claim 63, wherein said memory is used as a frame memory for luminance/chrominance separation of said channel-demodulated analog television signal, in said analog video mode.

65. A receiver according to claim 59, wherein said analog processing means performs post-processing of said channel-demodulated analog television signals.

66. A receiver according to claim 65, wherein said memory is used as a frame memory for post-processing of said channel-demodulated analog television signal, in said analog video mode.

67. A receiver according to claim 59, wherein said analog processing means performs luminance/chrominance separation and post-processing said channel demodulated analog television signal.

68. A receiver according to claim 67, wherein said memory is used as a frame memory for luminance/chrominance separation and post-processing of said channel-demodulated analog television signal, in said analog video mode.

69. A method for receiving television signal analog-processed by a predetermined analog broadcasting method and television signal digital-processed by a predetermined digital signal format, comprising the steps of:

(a) generating a mode selection signal to determine whether a channel selected by a user is a television channel of an analog video mode or a television channel of a digital video mode;

(b) storing digital television signal received according to said mode selection signal in a memory for digital video decoding, and decoding using the data stored in said memory.

70. A method for receiving television signal analog-processed according to a predetermined analog broadcasting method and television signal digital-processed by a predetermined digital signal format, comprising the steps of:

(a) generating a mode selection signal to determine whether a channel selected by a user is a television channel of an analog video mode or a television channel of a digital video mode;

(b) storing analog television signal received according to said mode selection signal in a mem-

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ory for digital video decoding, and reading the data stored in said memory to process the data in said memory in said analog video mode.

71. A method for receiving television signal analog-processed according to a predetermined analog broadcasting method and television signal digital-processed by a predetermined digital signal format, comprising the steps of:

(a) generating a mode selection signal to determine whether a channel selected by a user is a television channel of an analog video mode or a television channel of a digital video mode;

(b) storing received digital television signal according to said mode selection signal in a memory for digital video-decoding and decoding the data stored in said memory in said digital video mode, and storing received analog television signal in said memory for digital video-decoding and reading the data stored in said memory to process the data in said memory in said analog video mode.

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FIG.1 (PRIOR ART)

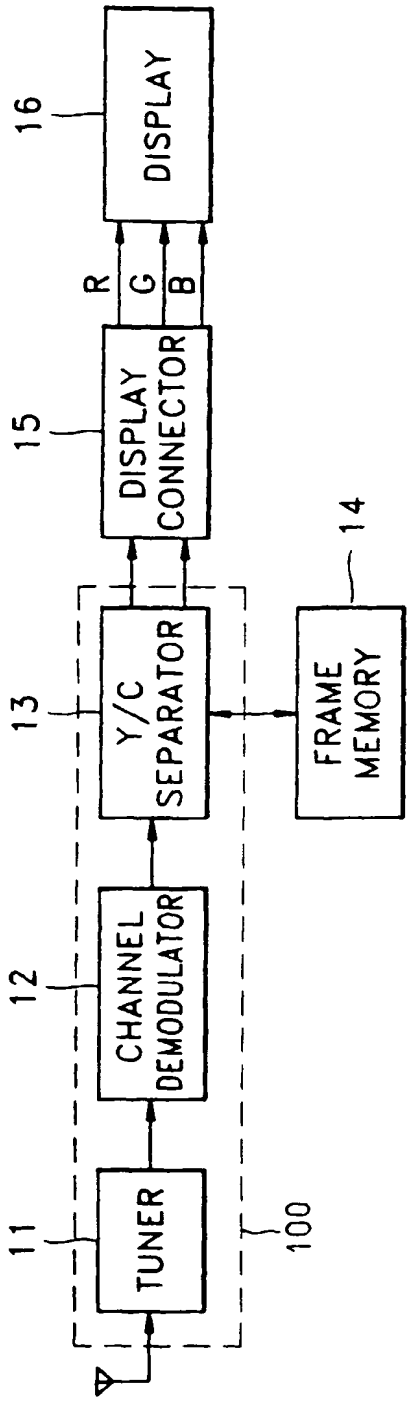

FIG.2 (PRIOR ART)

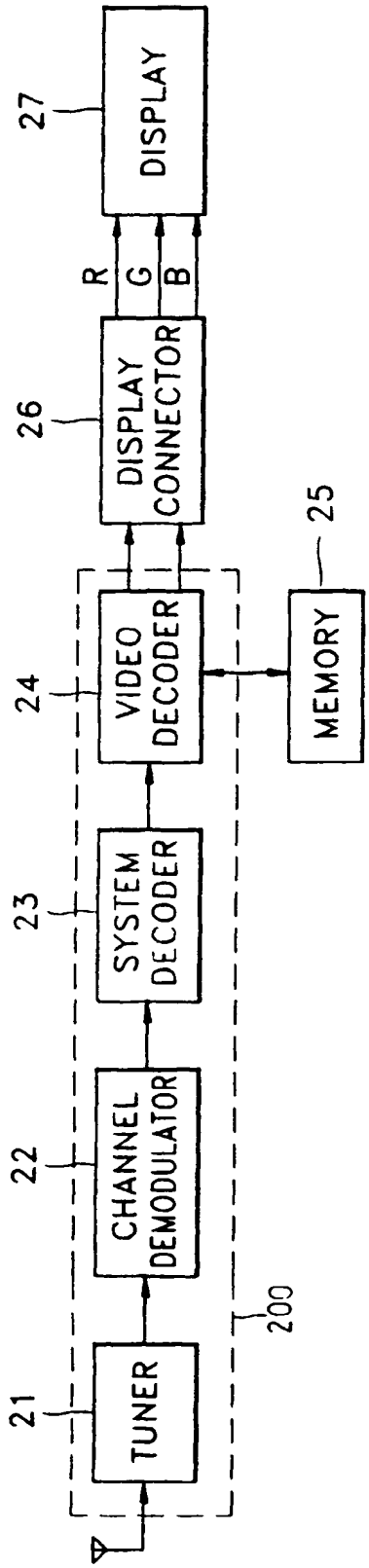

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FIG. 3 (PRIOR ART)

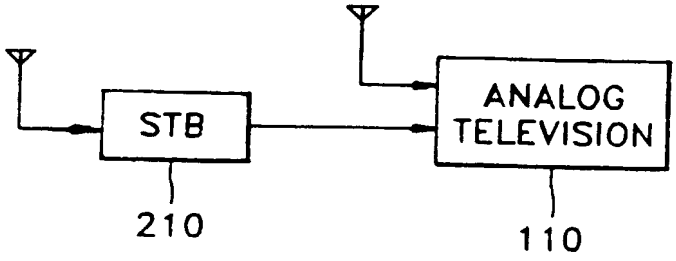

FIG. 4 (PRIOR ART)

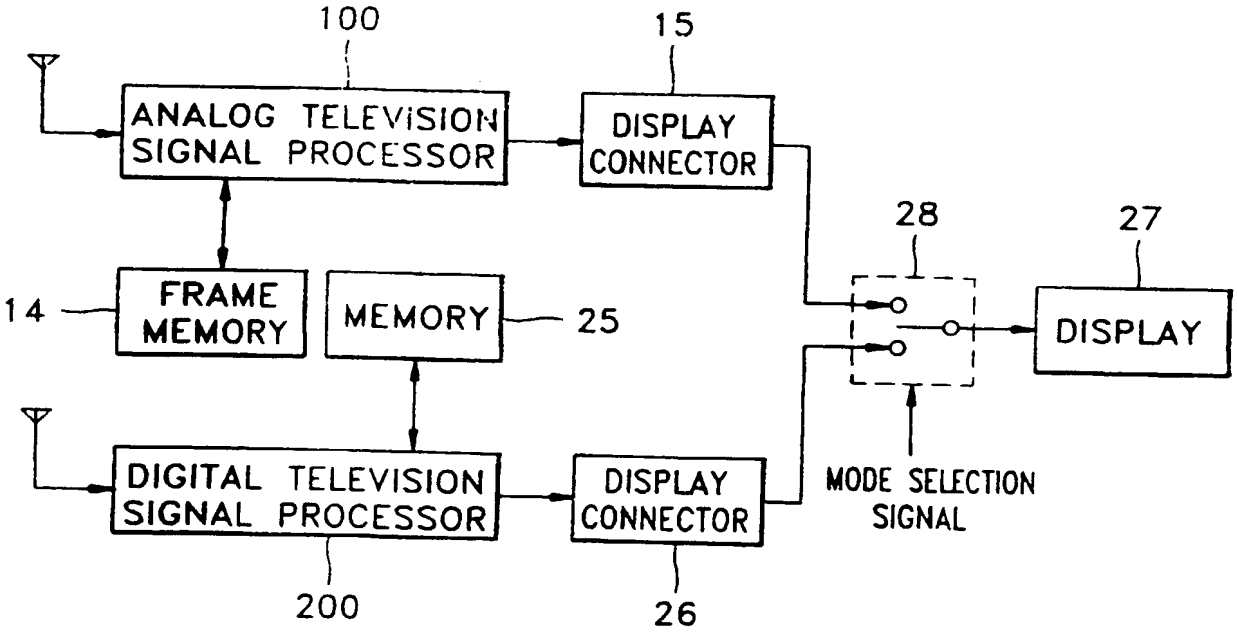

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FIG. 5

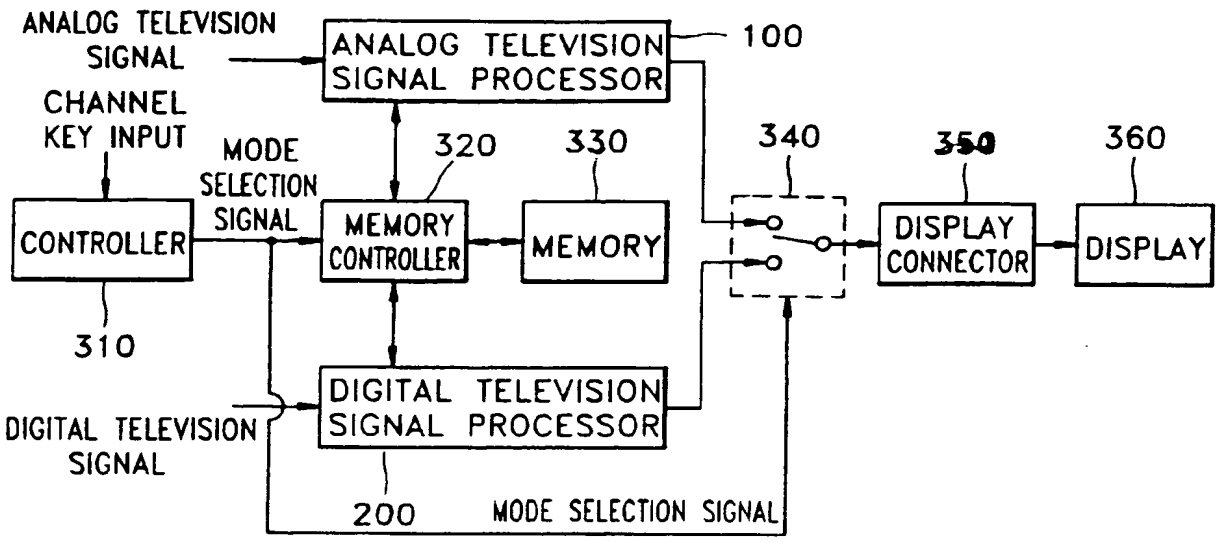

FIG. 6

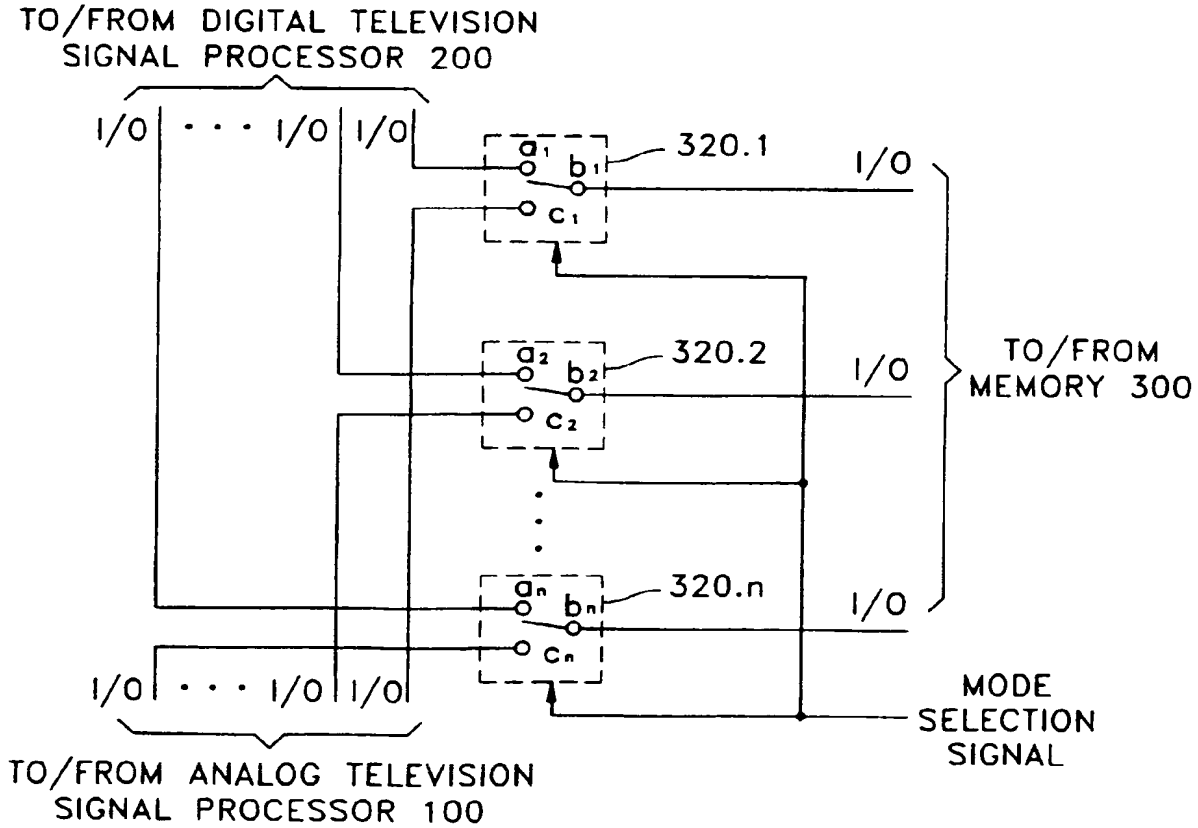

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FIG. 7

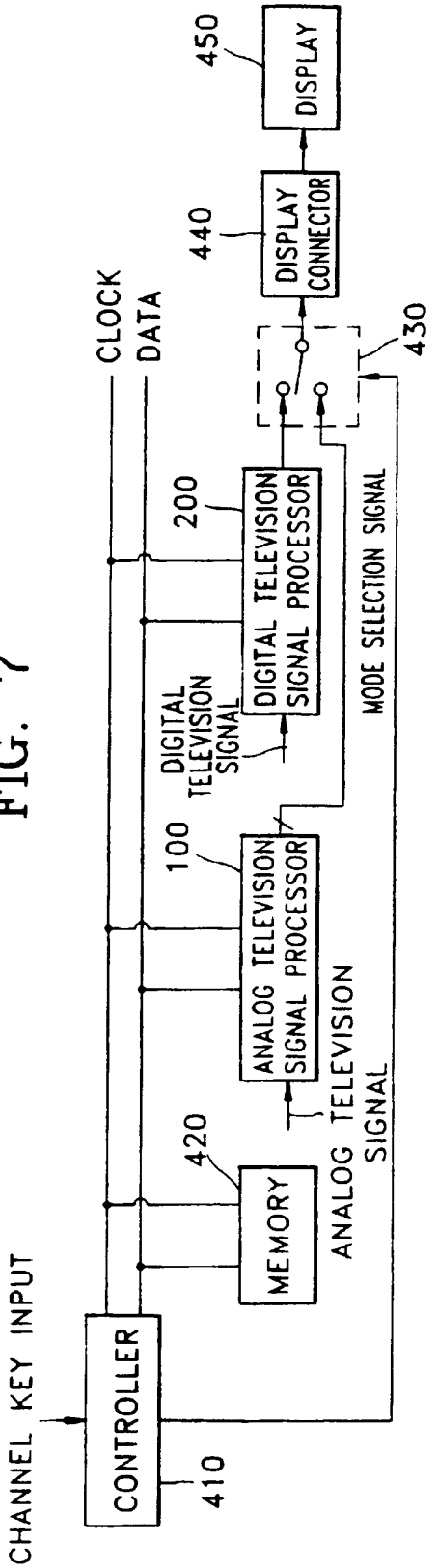
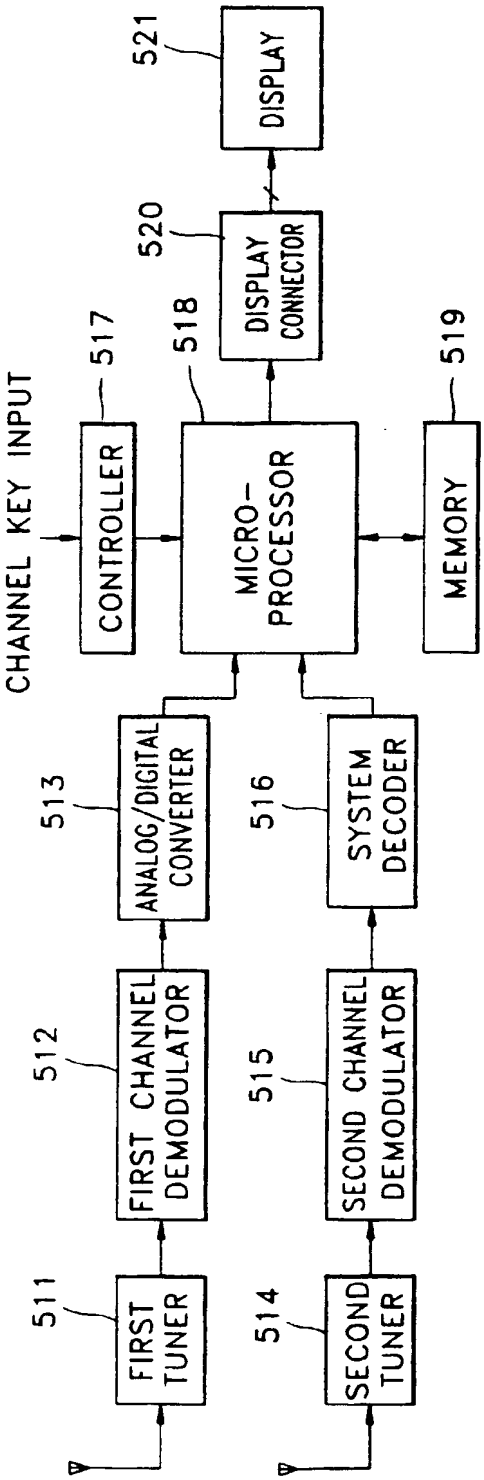


FIG. 8



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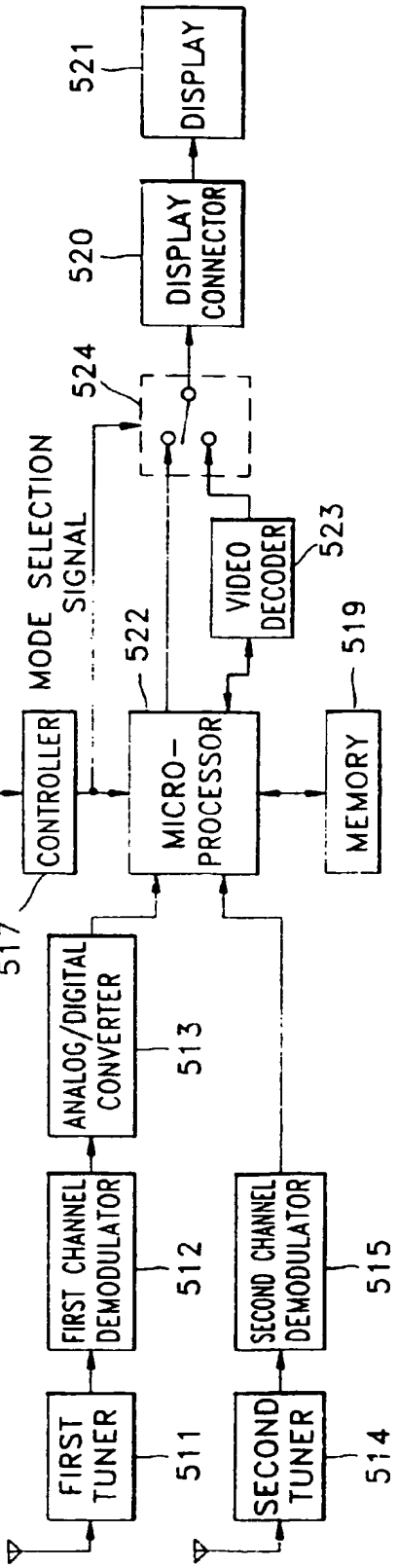

FIG. 9A

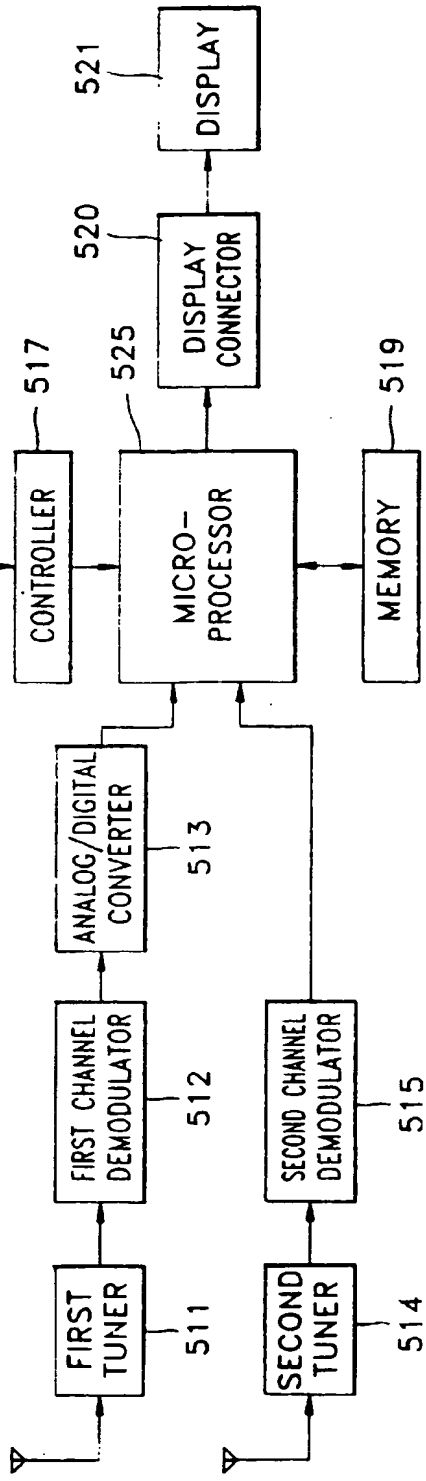

FIG. 9B

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FIG. 9C

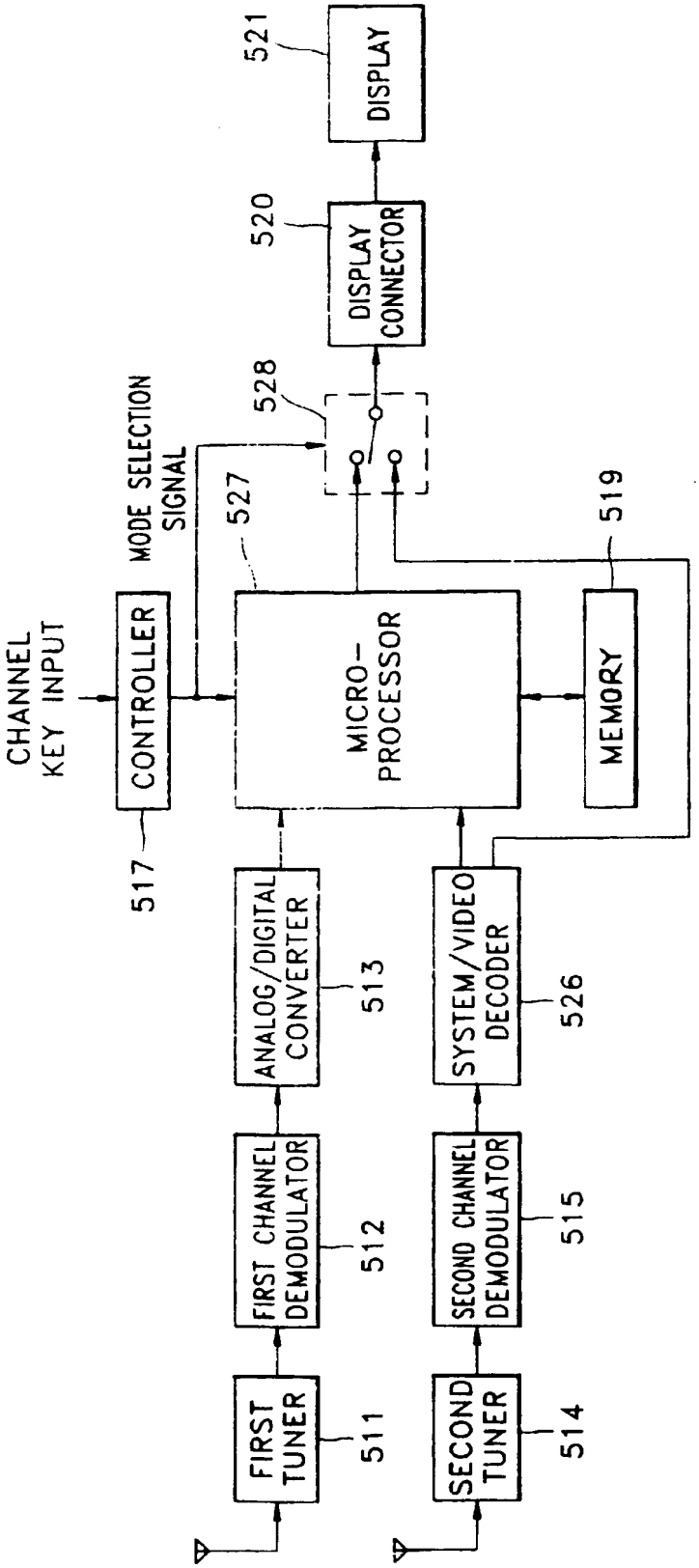

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FIG. 10

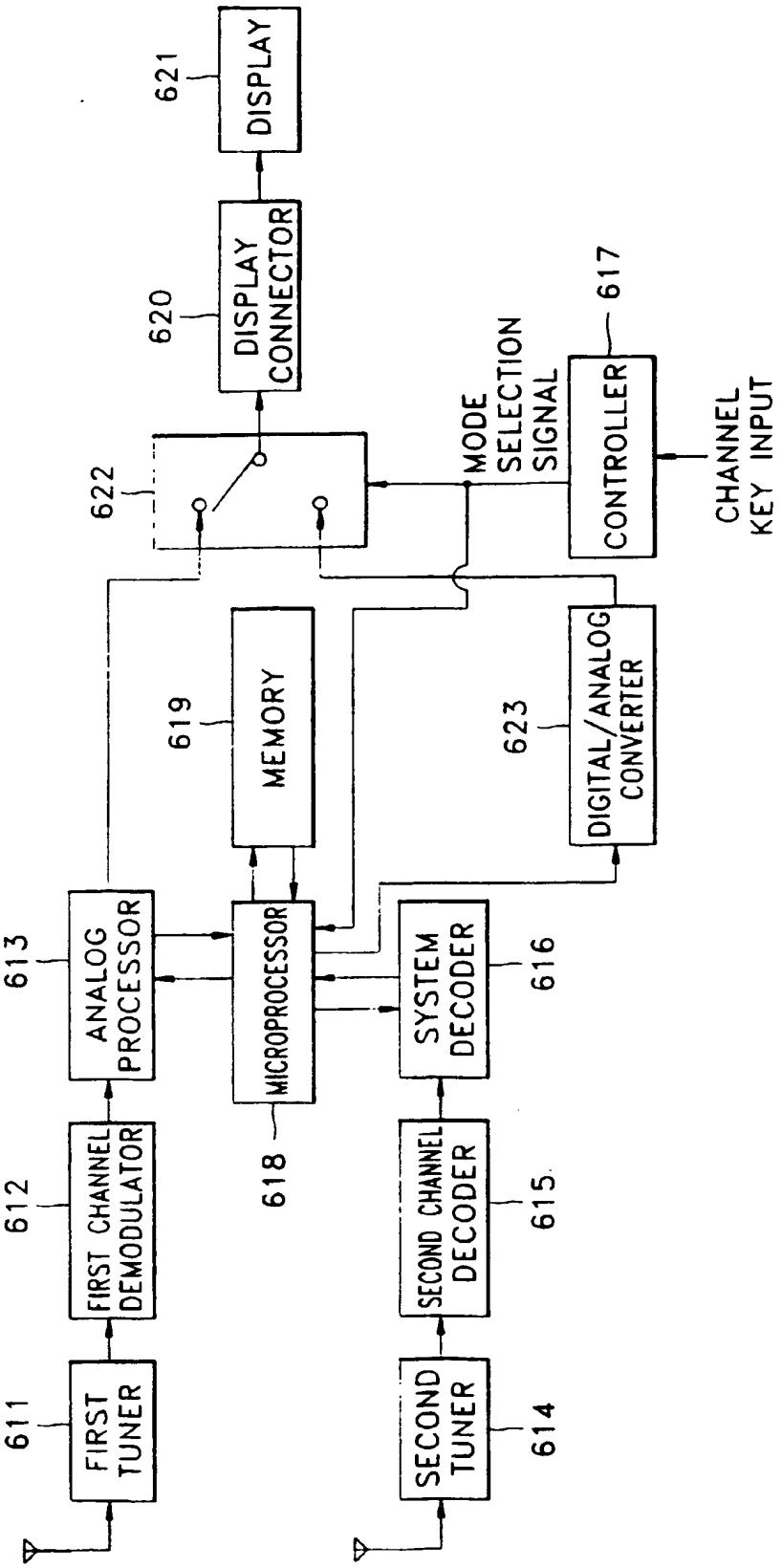

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FIG. 11

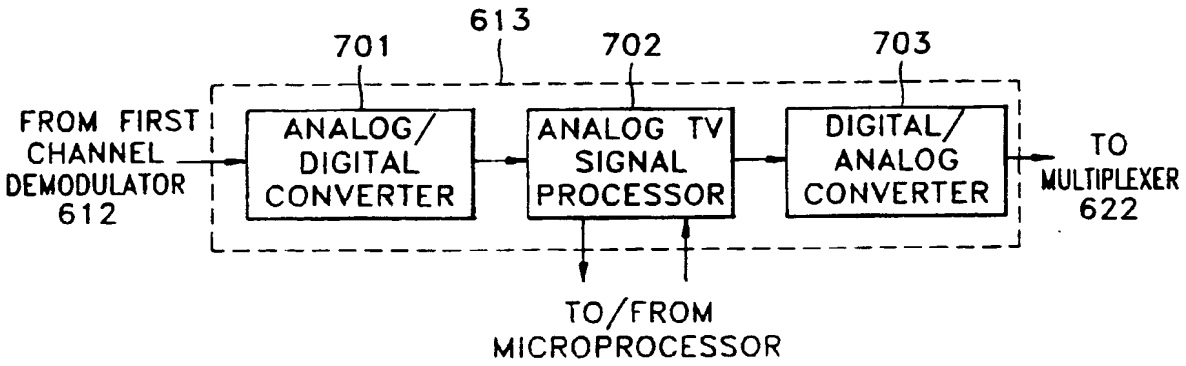

FIG. 12A

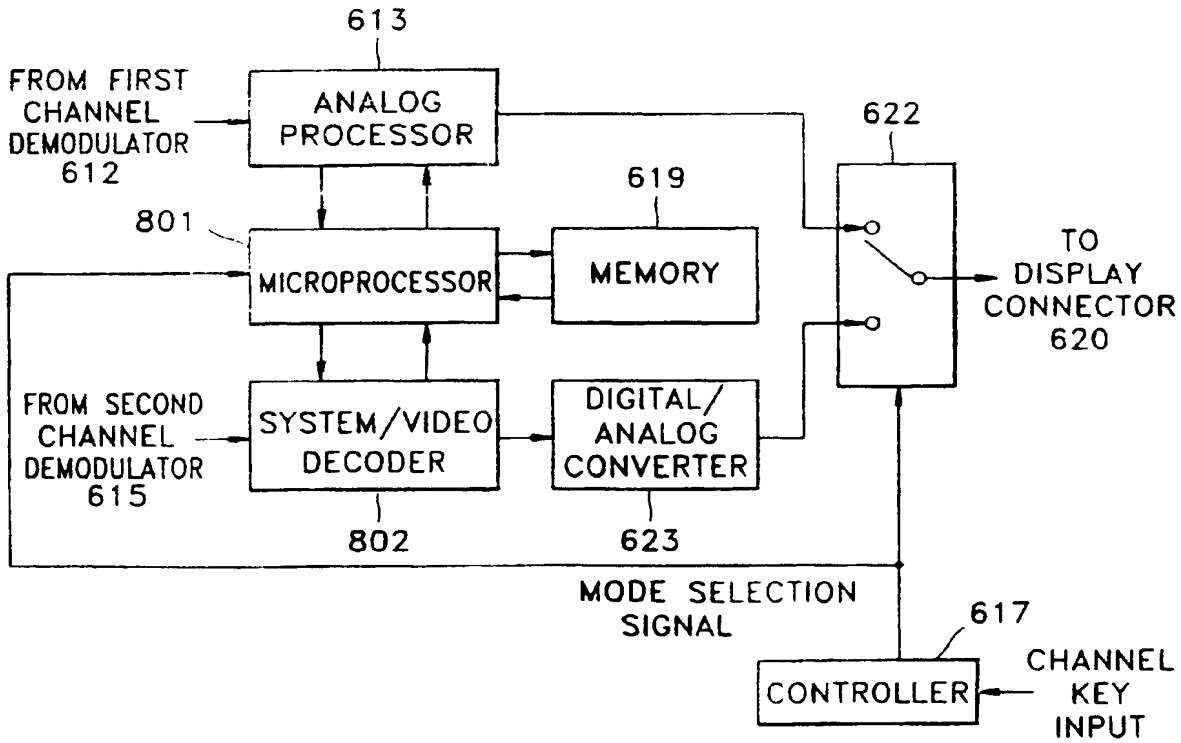

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FIG. 12B

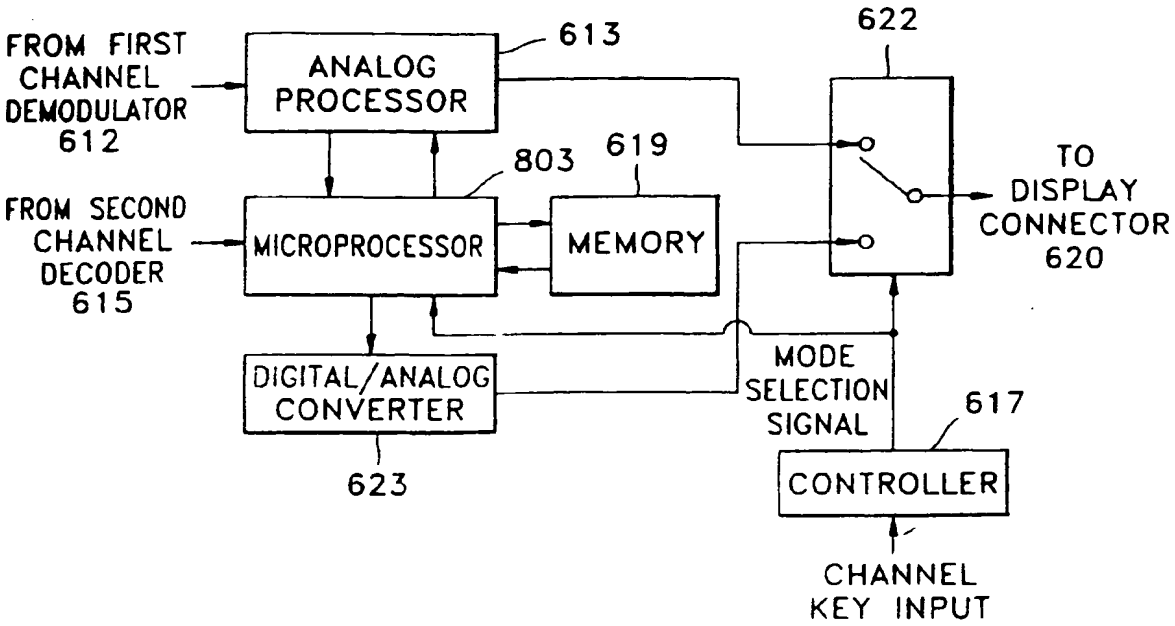
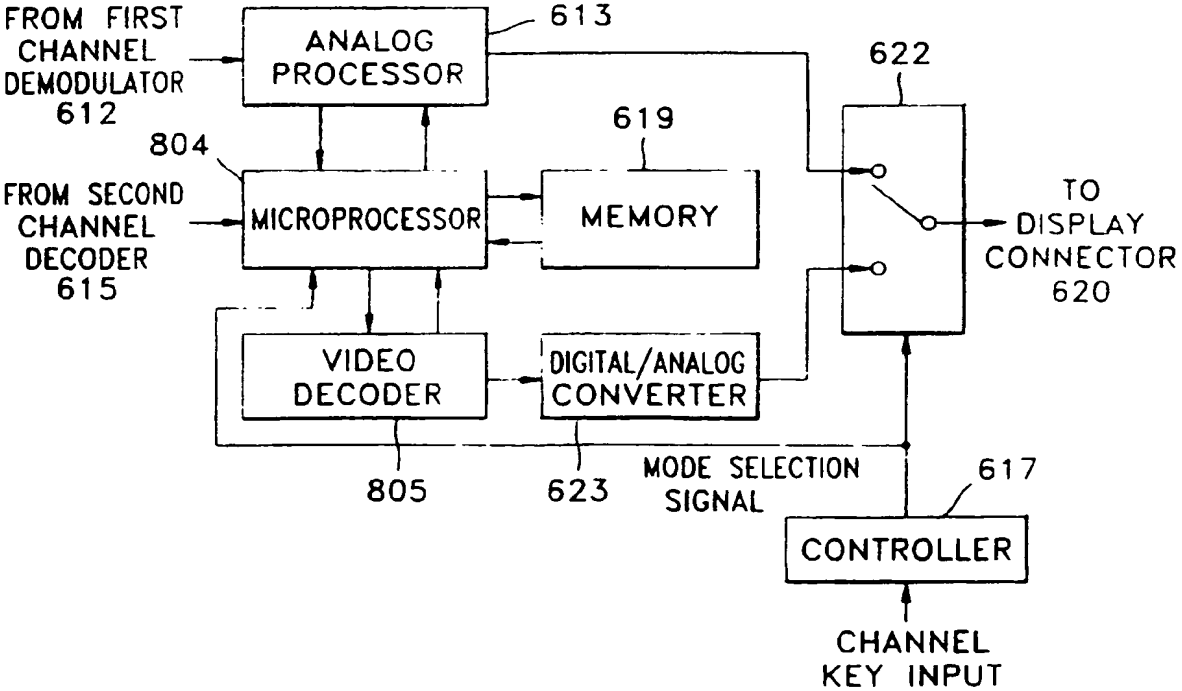


FIG. 12C



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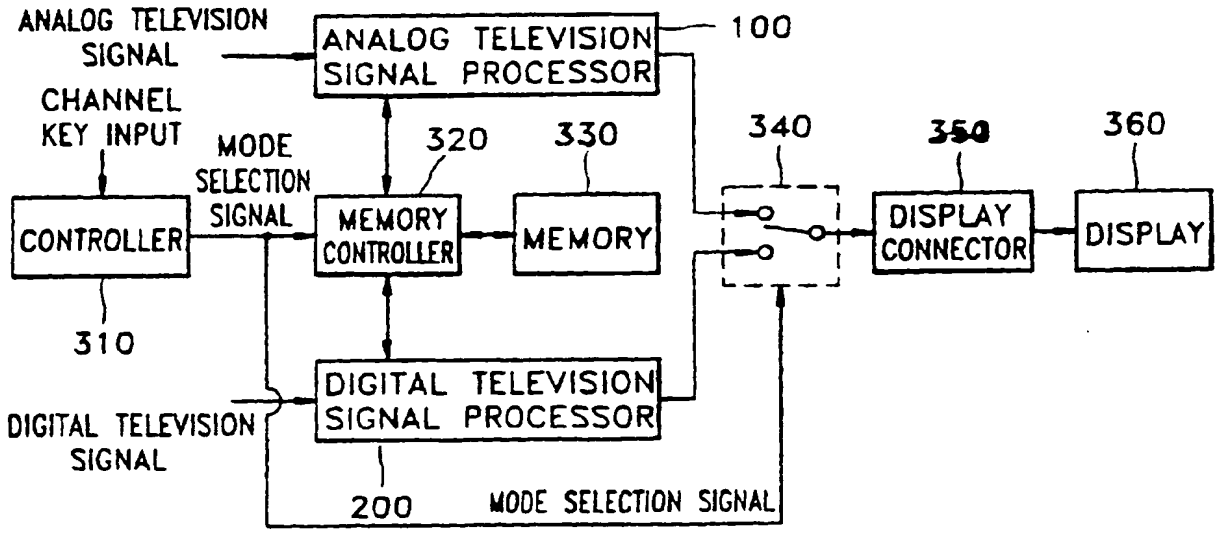
(54) Receiver having analog and digital video modes and receiving method thereof

(57) In a receiver having both an analog video service mode and a digital video mode and a receiving method thereof, when the analog video mode is selected according to a mode selection signal indicating that a television channel is for the analog video mode or the digital video mode, a large-capacity memory used for the digital video-decoding may also be used as a frame memory for Y/C separation and post-processing, for enhancing picture quality, improving the efficiency of the memory and reducing the cost of a system.

FIG. 5



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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 30 6707

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 574 273 A (TOKYO SHIBAURA ELECTRIC CO ;TOSHIBA AVE KK (JP)) * abstract * * columr 11, line 1 - line 54; figure 6 * ---	1,2,6-8, 12, 16-18, 31,37, 38,43, 46,48, 50,59, 60,69-71	H04N5/44 H04N5/46
A	US 5 448 300 A (YAMADA MASAHIRO ET AL) * abstract * * column 4, line 58 - column 7, line 29; figures 1,2 * ---	1,2,6-8, 12, 16-18, 31,37, 38,43, 46,48, 50,59, 60,69-71	
A	EP 0 619 675 A (IBM) * abstract * * column 4, line 25 - column 5, line 21; figure 2 * -----	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 January 1998	Fuchs, P

CATEGORY OF CITED DOCUMENTS

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